

### Remarks

Claims 1-3, 5-11 and 14-20 are pending, and claims 1-3, 5-11 and 14-20 stand rejected. The Applicants respectfully traverse the rejection and request allowance of claims 1-3, 5-11 and 14-20.

### § 102 Claim Rejections

The Examiner rejected claims 1-3, 5, 10, 11, 14, 15, and 20 under 35 U.S.C. § 103 in view of U.S. Patent number 6,018,515 (Sorber) in further view of U.S. Patent number 6,304,578 (Fluss). The Applicants submit that claims 1-3, 5, 10, 11, 14, 15, and 20 are novel and non-obvious over Sorber, Fluss, or any combination thereof in light of the following remarks.

Independent claim 1 claims a memory controller having the limitation of: *"if occupancy on a first transmit buffer corresponding with a first transmit channel exceeds a threshold, then prioritize the transmit channels to transmit packets from the first transmit buffer corresponding with the first transmit channel"*. The Applicants submit that Sorber does not teach a memory controller as claimed in claim 1, and the Examiner agreed with the Applicants in the Office action. See Office action, page 3.

To reject the memory controller of claim 1, the Examiner relied on the teaching in Fluss. In Fluss, a headend (103) includes a plurality of queues (105-107) for a plurality of shared data channels. See Fluss, FIG. 1, column 4, lines 21-33. One queue services each data channel. See Fluss, FIG. 1, column 4, lines 34-36. The queue stores a number of packets which have not yet been routed to users of the data channel. See Fluss, column 4, lines 36-39. The headend determines which priority scheme to apply to the data packets in the queue. See Fluss, FIG. 1, column 4, lines 55-58. The priority scheme determines which data packets are transmitted from the queue of the data channel to a user. See Fluss, FIG. 1, column 4, lines 58-60. If a queue is filled to a critical value, then the headend assigns a new priority to the packets in the queue. See Fluss, FIG. 1, column 5, lines 4-6. The priority is used to determine which order to transmit the packets out of the queue. See Fluss, FIG. 1, column 5, lines 4-8. The highest priority goes to control protocol packets (e.g., control protocol packets are transmitted out of the queue first). See Fluss, FIG. 1, column 5, lines 17-20. Then the size of the packets is evaluated. See Fluss, FIG. 1, column 5, lines 22-23. The largest packets are given a higher priority than smaller

packets. See Fluss, FIG. 1, column 5, lines 23-28.

Fluss does not teach a memory controller that “prioritize[s] the transmit channels to transmit packets from the first transmit buffer corresponding with the first transmit channel” if the occupancy on a first transmit buffer corresponding with a first transmit channel exceeds a threshold as described in claim 1 of the pending application. Fluss prioritizes *packets* of a channel and treats packets within a queue differently based on the assigned priority. As described above, in Fluss, the control protocol packets are transmitted first out of the queue, then the larger packets, then the small packets, etc. FIG. A below illustrates a queue filled with packets as described in Fluss.

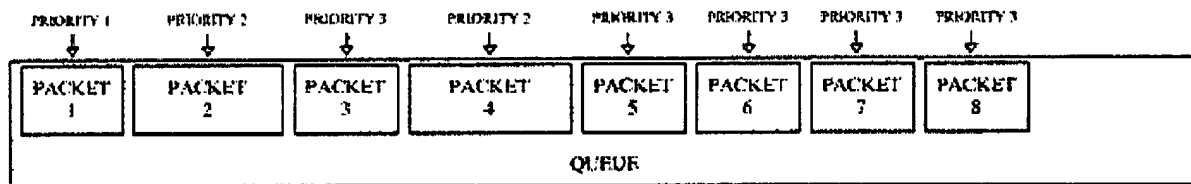


FIG. A

According to Fluss, each packet is prioritized according to the priority scheme. Assume that packet 1 is a control protocol packet. Packet 1 is given a priority of 1 and transmitted first. Assume that packets 2 and 4 are large packets. Packets 2 and 4 are given a priority of 2 and transmitted next. Assume packets 3 and 5-8 are small packets. Packets 3 and 5-8 are given a priority of 3 and transmitted next. The packets within the queue are each given a priority and are treated differently based on the given priority.

In contrast, the memory controller in claim 1 prioritizes a *channel* and its corresponding buffer, not the individual packets within the buffer. The memory controller in claim 1 does not need to look at each individual packet in a transmit buffer and assign a priority to each individual packet as in Fluss. The memory controller in claim 1 assigns a priority to channels having buffers that exceed a threshold. The memory controller of claim 1 may treat all packets in the buffer the same, as the memory controller operates on a channel-level and not the packet-level. FIG. B below illustrates a plurality of buffers for a plurality of channels as in claim 1.

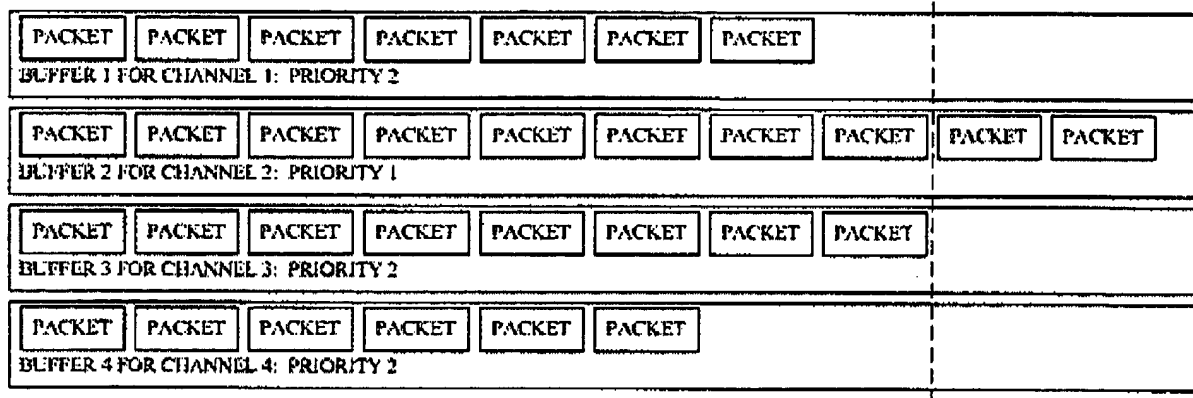


FIG. B

FIG. B shows four buffers for four channels in one example. The dotted line in FIG. B illustrates the threshold for each buffer. Assume that buffer 2 has exceeded the threshold, and buffers 1 and 3-4 have not exceeded the threshold. Because buffer 2 has exceeded the threshold, the channel for buffer 2 is given a priority 1 and the channels for buffers 1 and 3-4 are given a priority 2. Based on the priorities given to the channels, buffer 2 may be emptied first to prevent buffer 2 from overrunning. The packets in the individual buffers 1-4 are not given different priorities as in Fluss, but the buffers for the channels are given a priority. Therefore, the Applicants submit that Fluss does not teach the memory controller as provided in claim 1.

Based on the above remarks, the Applicants submit that claim 1 is novel and non-obvious in view of Sorber, Fluss, and any combination thereof. The same arguments apply for claims 2-3, 5, 10, 11, 14, 15, and 20.

### § 103 Claim Rejections

The Examiner rejected claims 6-9 and 16-19 under 35 U.S.C. § 103 in view of Sorber, Fluss, and U.S. Patent number 5,007,051 (Dolkas). The Applicants submit that claims 6-9 and 16-19 are novel and non-obvious for the reasons provided above.

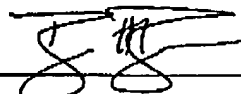
### Conclusion

Based on the above remarks, the Applicants submit that claims 1-3, 5-11 and 14-20 are

allowable. There may be additional reasons in support of patentability, but such reasons are omitted in the interests of brevity. The Applicants respectfully request allowance of claims 1-3, 5-11 and 14-20.

Any fees may be charged to deposit account 502622.

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**SIGNATURE OF PRACTITIONER**

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